IN THE DRAWINGS

Please replace Figures 2-4 as indicated in the attached replacement sheets.

REMARKS

This response is intended as a complete response to the Office Action dated June 1, 2005. In view of the following discussion, the Applicants believe that all claims are in allowable form.

ELECTION OF CLAIMS

The Applicants confirm the election of claims 1-23 without traverse. Claims 24-28 have been cancelled without prejudice. Applicants reserve the right to file continuing and/or divisional applications to prosecute the non-elected subject matter.

PRIORITY

The Applicants thank the Examiner for his comments regarding the possible benefits under 35 U.S.C. § 119(a)-(d).

SPECIFICATION

The Applicants hereby amend paragraphs **[0018]**, **[0040]**, **[0054]**, **[0055]**-**[0056]**, and **[0058]** to correct minor errors. The Applicants submit that no new matter has been entered by these amendments.

DRAWINGS

The Applicants hereby amend Figures 2-4 to correct minor errors. Specifically, Figure 2 has been amended to correct reference numeral 212; Figure 3 has been amended to correctly show features 332 and 334 in broken lines as described in the specification; and Figure 4 has been amended to add reference numerals 418 and 428 to the distributions plotted in Figures 4A and 4B, respectively. The Applicants submit that no new matter has been entered by these amendments.

CLAIMS

Claims 14 and 22 have been amended to correct dependency and a typographical error, respectively. The Applicants submit that these amendments were made for reasons unrelated to patentability and that no new matter has been added.

CLAIM REJECTIONS

A. Double Patenting Claims 1 and 7-10

Claims 1 and 7-10 stand provisionally rejected under the judicially created doctrine of obviousness-type double-patenting as being unpatentable over claims 8-9, 11, and 13-14 of copending United States Patent Application No. 10/690,318 filed Oct. 21, 2003 (United States Patent Application Publication No. 2005/0085090) to *Mui et al.* (hereinafter *'318*). The Applicants respectfully disagree.

Claim 8 of '318 recites:

> A method for controlling accuracy and repeatability of an etch process, comprising:
> (a) providing a batch of substrates, each substrate having a patterned mask formed on a film stack comprising at least one material layer;
> (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates;
> (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b);
> (d) etching the at least one material layer on the at least one substrate;
> (e) measuring dimensions of etched structures formed on the at least one substrate during step (d); and
> (f) adjusting the process recipe of step (c) or/and the process recipe of step (d) based on the measurements performed at step (e).

As such, *'318* teaches to measure the patterned mask (step b) and trim the patterned mask using a process recipe based on the measurements performed at step (b) (step c). '318 further teaches to subsequently etch and measure the etched structures in layers beneath the patterned mask (steps d and e). Finally, '318 teaches to adjust the mask trimming process recipe of step (c) and/or the etch process recipe of step (e) based upon the measurements of the etched structures taken at step (e).

Therefore, *'318* teaches adjusting the process of trimming the patterned mask based upon either measurements taken of the patterned mask (step b) or the etched

structures (step e), or adjusting the process of etching the structures based upon measurements of the structures themselves and not the patterned mask. Claims 9, 11, 13-14 depend from claim 8 and relate to a means for performing such a method.

In contrast, Applicants' independent claim 1, as amended, teaches a method comprising steps of measuring dimensions of elements of a patterned mask and, based of results of these measurements, adjusting a process recipe for an overetch step of an etch process that forms the structures on a substrate (*i.e.*, beneath the patterned mask). Claims 7-10 depend, directly or indirectly, from claim 1 and recite additional features therefor. *'318* fails to teach or suggest measuring dimensions of elements of the mask on the substrate and adjusting a process recipe for an overetch step of the etch process using the results of measuring said dimensions, as recited in claim 1.

Thus, Applicants submit that claims 1 and 7-10 are patentably distinct from and not anticipated by claims 8-9, 11, and 13-14 of *'318* and are fully compliant with provisions of the judicially created doctrine of obviousness-type double-patenting. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

B. Double Patenting Claims 12 and 19-23

Claims 12 and 19-23 stand provisionally rejected under the judicially created doctrine of obviousness-type double-patenting as being unpatentable over claims 16-17, 19, 21, and 23-27 of *'318*. The Applicants respectfully disagree.

In claims 16-17, 19, 21, and 23-27, *'318* teaches substantially the same method as discussed in reference to claims 8-9, 11, and 13-14 above in section A. However, in claims 16-17, 19, 21, and 23-27, a layer beneath the patterned mask is specifically identified as a gate electrode layer of a transistor.

Correspondingly, Applicants' independent claim 12, as amended, teaches a process comprising steps of measuring dimensions of elements of a patterned mask and, based of results of these measurements, adjusting a process recipe for an overetch step of an etch process that forms a gate structure of a transistor beneath the

patterned mask. Claims 19-23 depend, directly or indirectly, from claim 12 and recite additional features therefore.

As such, at least for the same reasons as discussed above in Section A, the Applicants submit that claims 12 and 19-23 are patentably distinct from claims 16-17, 19, 21, and 23-27 of *'318* and are fully compliant with provisions of the judicially created doctrine of obviousness-type double-patenting. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

C. 35 U.S.C. §102(e) Claims 1-13, 15, and 17-23

Claims 1-13, 15, and 17-23 stand rejected as being anticipated by United States Patent No. 6,620,631 B1 issued Sep. 16, 2003 to *Tao et al.* (hereinafter *Tao*). In response, the Applicants have amended claims 1 and 12 to more clearly recite aspects of the invention.

Independent claim 1, as amended, recites limitations not taught, shown, or suggested by *Tao*. *Tao* teaches an etch method where parameters of a single-step plasma etch process of forming structures 12a-12e in a target layer 12 are adjusted based on measurements of linewidths of respective patterned masking layers 14a-14e. *Tao* discloses that adjustable parameters include at least one plasma etch parameter, specifically, an etchant gas flow rate, chamber pressure, plasma power, pre-etch trimming of the masking layers 14a-14e, and pre-etch depositions on sidewalls of the masking layers 14a-14e (col. 9, lines 15-30;col. 10, lines 9-28).

However, *Tao* fails to teach or suggest an etch method comprising the step of adjusting a process recipe for an overetch step of an etch process that forms the structures on a substrate, as recited in claim 1.

More specifically, in contrast with *Tao*, claim 1 recites using an etch process having an overetch step (*i.e.*, a multi-step etch process) and adjusting the process recipe for the overetch step, thereby controlling dimensions of the structures being etched. Therefore, *Tao* does not teach Applicants' invention.

Independent claim 12, as amended, recites similar subject matter and, additionally, identifies the being etched layers beneath the patterned etch mask as the

layers of a gate structure of a field effect transistor. As such, claim 12 is patentable over Tao at least for the same reasons as discussed above in reference to claim 1.

Support for the amendments may be found in the specification at least at paragraphs [0034]-[0037].

Furthermore, claims 2-11, 13, 15, and 17-23 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since *Tao* does not anticipate or make obvious Applicants' invention as recited in claims 1 and 12, dependent claims 2-11, 13, 15, and 17-23 are also patentable over *Tao*.

Thus, Applicants submit that independent claims 1 and 12 and claims 2-11, 13, 15, and 17-23 depending therefrom are patentable over *Tao*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

D. 35 U.S.C. §103(a) Claim 14

Claim 14 stands rejected as being unpatentable over *Tao* in view of Wolf, *Silicon Processing for the VLSI Era*, Vols. 1 and 4, Lattice Press (1986, 2002) (hereinafter referred to as "*Wolf*") and Streetman, *Solid State Electronic Devices*, Pretice Hall (1990) (hereinafter referred to as "*Streetman*"). In view of the amendments to claim 12, from which claim 14 depends, the Applicants respectfully disagree.

Independent claim 12, as amended, recites limitations not taught, shown, or suggested by a combination of *Tao, Wolf*, and *Streetman*. The patentability of claim 12 over *Tao* has been discussed above in Section C. *Wolf* teaches that refractory silicides and high-k dielectrics may be used as gate electrode materials and gate dielectrics, respectively (vol. 1, p. 385; v. 4, pp. 145-146); and *Streetman* teaches gate dielectrics formed from SiO_2 (p. 300).

However, neither *Wolf* nor *Streetman* teaches or suggests an etch method comprising the step of adjusting a process recipe for an overetch step of an etch process that etches a layer of a film stack of a gate structure of a transistor, as recited in claim 12. As such, the teachings of *Wolf* and *Streetman* may not be utilized to modify the method of *Tao* in a manner that yields the limitations recited in claim 12. As such, a *prima facie* case of obviousness has not been established as the combination

of the cited references fails to yield all of the limitations recited in claim 12, from which claim 14 depends.

Thus, the Applicants submit that claim 14 is patentable over *Tao* in view *Wolf* and *Streetman*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

E. 35 U.S.C. §103(a) Claim 16

Claim 14 stands rejected as being unpatentable over *Tao* in view of *Wolf* and *Streetman* and in further view of United States Patent No. 5,858,847 issued Jan. 12, 1999 to *Zhou et al.* (hereinafter referred to as "*Zhou*"). In view of the amendments to claim 12, from which claim 14 depends, the Applicants respectfully disagree.

Independent claim 12, as amended, recites limitations not taught, shown, or suggested by any combination of *Tao, Wolf, Streetman,* and *Zhou*. The patentability of claim 12 over the combination of *Tao, Wolf*, and *Streetman* has been discussed above in Section D. *Zhou* teaches a method of fabricating a drain structure of a field effect transistor that uses a hard mask formed from SiON, SiO_2, or Si_3N_4 (col. 4, lines 40-45).

However, *Zhou* fails to teach or suggest an etch method comprising the step of adjusting a process recipe for an overetch step of an etch process that etches a layer of a film stack of a gate structure of a transistor, as recited in claim 12. As such, the teachings of *Zhou* may not be utilized to modify the method of *Tao*, alone or in combination with *Wolf* and *Streeman*, in a manner that yields the limitations recited in claim 12. As such, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield all of the limitations recited in claim 12, from which claim 16 depends..

Thus, the Applicants submit that claim 16 is patentable over *Tao* in view *Wolf*, *Streetman*, and *Zhou*. Accordingly, the Applicants respectfully request the rejection be withdrawn and the claims allowed.

NEW CLAIMS

New claims 29-33 have been added to the application. Claims 29-31 depend, directly or indirectly, from claim 1. Claims 32-33 depend, directly or indirectly, from claim 12. The Applicants submit that no new matter has been added and that these claims are allowable at least for the reasons detailed above. Furthermore, claims 29, 30, and 32 recite measuring the dimensions of elements of the mask on the substrate in a number of regions (at least five regions in claim 30). In addition, claims 31 and 33 recite mathematically processing the measurements from the number of regions to create the result utilized in the adjusting step. The Applicants submit that these additional limitations are further not taught or suggested in the cited prior art. Accordingly, the Applicants request allowance of these claims.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

9/1/05

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